

Appl. No. 10/056,367  
Amdt. dated 2/23/2004  
Reply to Office Action of November 7, 2003

PATENT

### REMARKS/ARGUMENTS

Claims 1-31 are pending in the present patent application. Claims 1, 6, 16, and 29-31 were rejected. Claims 1, 16, and 29 have been amended. No new matter has been added to the amended claims. Reconsideration of the amended claims is respectfully requested.

#### Allowed Claims

Claims 2-5, 7-15, and 17-28 have been allowed.

#### Rejected Claims

Claims 1, 6, 16, and 29-31 were rejected as being anticipated by U.S. Patent 6,023,175 to Nunomiya et al.

As shown in Figure 1 of Nunomiya, the input signal received by the level interface circuit is a single-ended signal. The level interface circuit requires a reference voltage in order for it to operate. There is no common mode component between the input signal and the reference voltage. See Nunomiya Col. 2, lines 43-53.

In contrast, the amplifier circuits of the present invention are designed to receive differential input signals. For example, differential input signals INA and INB are shown in the Figures of the present application. Input signals INA and INB have a common mode relationship.

An input buffer of the present invention can receive differential input signals according to multiple differential I/O standards. Different I/O standards can have different input operating ranges.

The input buffer has two differential amplifier circuits. Each differential amplifier operates at a different common mode input operating range during a selected input buffer mode.

Claim 1 has been amended to include the following language:

a first digital I/O standard that has a first input operating range, wherein a common mode component of the first and second input signals is in the first input operating range during a first input buffer mode  
second digital I/O standard that has a second input operating range greater than the first input operating range, wherein the common mode component of the first and

Appl. No. 10/056,367  
Amdt. dated 2/23/2004  
Reply to Office Action of November 7, 2003

PATENT

second input signals is in the second input operation range during a second input buffer mode;

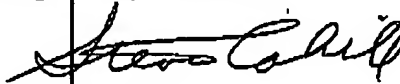
Nunomiya et al. does not disclose or suggest these features of amended claim 1.  
Amended claims 16 and 29 are allowable for similar reasons.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



Steven Cahill  
Reg. No. 44,578

TOWNSEND and TOWNSEND and CREW LLP  
Two Embarcadero Center, Eighth Floor  
San Francisco, California 94111-3834  
Tel: 650-326-2400 Fax: 415-576-0300  
60137432 v1